We claim:

1. An over-programming condition detector for use with an array of multistate memory cells, each cell programmable to store an amount of electric charge representative of a desired state selected from at least four sequential data states, the detector comprising:

a first logic gate for detecting a first one of the sequential data states in data intended to be written to the array;

a second logic gate for detecting a second one of the sequential data states in data intended to be written to the array;

a third logic gate for detecting a third one of the sequential data states in data intended to be written to the array; and

a fourth logic gate for receiving data written to the array.

2. The detector of claim 1, wherein each logic gate is an AND gate.

3. An over-programming condition detector for use with an array of multistate memory cells, each cell programmable to store an amount of electric charge representative of a desired state selected from at least four sequential data states, the detector comprising:

a first logic gate for detecting a first one of the sequential data states in data intended to be written to the array;

a second logic gate for detecting a second one of the sequential data states in data intended to be written to the array;

a third logic gate for detecting a third one of the sequential data states in data intended to be written to the array;

a fourth logic gate coupled to the buffer and an output of the first logic gate for detecting a first over-programmed condition;

a fifth logic gate coupled to the buffer and an output of the second logic gate for detecting a second over-programmed condition; and

a sixth logic gate coupled to the buffer and an output of the third logic gate for detecting a third over-programmed condition.

4. The detector of claim 3, wherein each logic gate is an AND gate.

5. The detector of claim 3, further comprising a seventh logic gate coupled to respective outputs of the fourth, fifth, and sixth logic gates.

6. An over-programming condition detector for use with an array of multistate memory cells, each cell programmable to store an amount of electric charge representative of a desired state selected from at least four sequential data states, the detector comprising:

a first logic gate for detecting a first one of the sequential data states in data intended to be written to the array;

a second logic gate for detecting a second one of the sequential data states in data intended to be written to the array;

a third logic gate for detecting a third one of the sequential data states in data intended to be written to the array;

a fourth logic gate coupled to the buffer, an enable input, and an output of the first logic gate for detecting a first over-programmed condition;

a fifth logic gate coupled to the buffer, the enable input, and an output of the second logic gate for detecting a second over-programmed condition; and

a sixth logic gate coupled to the buffer, the enable input, and an output of the third logic gate for detecting a third over-programmed condition.

7. The detector of claim 6, wherein each logic gate is an AND gate.

8. The detector of claim 6, further comprising a seventh logic gate coupled to respective outputs of the fourth, fifth, and sixth logic gates.

9. A multistate memory system comprising:

an array of multistate memory cells, with each cell programmable to store an amount of electric charge representative of a desired state selected from at least four sequential data states;

a buffer for coupling to the array of multistate memory cells;

a memory programming module coupled to the buffer for programming each of the multistate memory cells to a desired one of the sequential data states; and

at least one over-programming condition detector coupled to the memory programming module for generating an over-programmed signal representative of one or more of the memory cells having been erroneously programmed to one of the sequential data states which is subsequent to the desired one of the sequential data states, wherein the over-programming condition detector comprises:

a first logic gate for detecting a first one of the sequential data states;

a second logic gate for detecting a second one of the sequential data states;

a third logic gate for detecting a third one of the sequential data states; and

a fourth logic gate coupled to the buffer.

10. The system of claim 9, wherein the memory programming module is configured to program each of the multistate memory cells to a desired state of at least four sequential data states.

11. The system of claim 9, wherein the memory programming module is configured to program multistate flash memory cells.

12. The system of claim 9, wherein each logic gate is an AND gate.